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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,019	10/05/2001	Myles H. Wakayama	47426/RJP/B600	3152

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EXAMINER	
KINKEAD, ARNOLD M	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,019	WAKAYAMA, MYLES H.	
	Examiner	Art Unit	
	Arnold M Kinkead	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/5/03 updated class/sub
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. ____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: ____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05-26-04 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 63-67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 63, last line, " the transistors" lacks proper antedcedent basis. The dependent claims 64-67 depend from claim 63 and thus are indefinite too.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 50-55, and 58-67 rejected under 35 U.S.C. 102(b) as being anticipated by Gersbach et al.(5,508,660 of record)

The reference by Gersbach et al discloses a CMOS charge pump that is part of a PLL loop(see figures 1 and 2). Figure 1 shows the PLL with detector(12) receiving input data, charge pump(14), and timing reference generator(18). In figure 4, first(H4) and second primary(H12) current sources are shown. The Gersbach et al reference meets the broad recitation for parallel current paths, the first path includes H4,H17(first current source at first end), H4,T17(second source at second end) . Note that the node 31 is between H17(first switch) and T17(second switch), for example.

The second path including H12,H3(first current source),H12,T14(second current source) and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point coupled to RC filter(on node 31).

The output node for the second path is coupled to the node with the capacitor(C). The adjusting current source formed in part by (T15,T4; and T12,T5). Also, a voltage difference being determined by the comparator op-amp with inherent trans-conductance to minimize current offsets. The method steps being inherent.

A first output node(31) and second output node(C) are shown. A filter(RC in general) is coupled to the first node and a capacitor C is shown in figure 4. A first output node(31) and second output node(49) are shown. A filter(RC in general) is coupled to the first node and a LOOP capacitor C is shown in figure 4. A feedback path is shown connected to reduce DC offset(note in col. 1, lines 48-60, The CMOS or transistors are part of the problem

due to the channel length modulation, i.e. parasitics(capacitive), that lead to the offset) at charge pump output. The adjustment current being developed by way of T4,T5. The method steps being inherent.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 56 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gersbach et al(US 5,508,660 cited by applicant).

The reference by Gersbach et al discloses a CMOS charge pump that is part of a PLL loop(see figures 1 and 2). Figure 1 shows the PLL with detector(12) receiving input data, charge pump(14), and timing reference generator(18). In figure 4, first(H4) and second primary(H12) current sources are shown. The Gersbach et al reference meets the broad recitation for parallel current paths, the first path includes H4,H17(first current source at first end), H4,T17(second source at second end) . Note that the node 31 is between H17(first switch) and T17(second switch), for example.

The second path including H12,H3(first current source),H12,T14(second current source) and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point coupled to RC filter(on node 31).

The output node for the second path is coupled to the node with the capacitor(C). The system that controls the value of the second current source includes the adjusting current source formed in part by (T15,T4; and T12,T5) coupled between the feedback means(amplifier) and the first and second current sources. Also, a voltage difference being determined by the comparator op-amp with inherent trans-conductance to minimize current offsets. The method steps being inherent.

A first output node(31) and second output node(C) are shown. A filter(RC in general) is coupled to the first node and a capacitor C is shown in figure 4. A first output node(31) and second output node(49) are shown. A filter(general RC, analog) is coupled to the first output node and a LOOP capacitor C is shown in figure 4. A feedback path(with amplifier) is shown connected to reduce DC offset(note in col. 1, lines 48-60, The CMOS or transistors are part of the problem due to the channel length modulation, i.e. parasitics(capacitive), that lead to the offset) at charge pump output. The adjustment current being developed by way of T4,T5. The method steps being inherent.

The reference does not describe a particular RC filter configuration, however, a series RC in parallel with another capacitor. This , however, is a conventional circuit used as a low pass filter for developing the VCO control signal, and is equivalent in function the general RC shown in Gersbach et al, that is, art recognized equivalent to provide a dc control signal for the VCO as is notoriously well known to one of ordinary skill in the art.

In light of the above it would have been obvious to one of ordinary skill in the art to have recognized that the general low pass filter of the Gersbach reference may be one of several notoriously well known RC configurations, functionally equivalent to the general RC filter shown in Gersbach et al, to allow for the control signal to be developed for the VCO this being well within the level of skill for one of ordinary skill in the art.

Response to Arguments

5. Applicant's arguments filed 05-26-04 have been fully considered but they are not persuasive. The examiner has considered applicant' s remarks about the first and second current paths having respective first and second output nodes with a filter coupled to said first output node and a capacitor coupled to the second output node.

The Gersbach et al reference meets the broad recitation for parallel current paths, the first path includes H4,H17(first current source at first end), H4,T17(second source at second end) the second path including H12,H3(first current source),H12,T14(second current source) and they have the same configuration(i.e. parallel) with corresponding feedback. The first output node for the first path include the point coupled to RC filter(on node 31).

The output node for the second path is coupled to the node with the capacitor(C). The adjusting current source formed in part by (T15,T4; and T12,T5). Also, a voltage difference being determined by the comparator op-amp with inherent trans-conductance to minimize current offsets. The method steps being inherent.

With regards the capacitor, figure 4 shows such a " dump" capacitor coupled to second output nodes of T17,T14 each transistor has a separate output tied to the capacitor. (note in col. 1, lines 48-60, The CMOS technology or transistors are part of the problem due to the channel length modulation, i.e. parasitics, that lead to the offset)

Also, the comparator (46) does determine a voltage difference that allows for the proper current mismatch to resolved.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner' s supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arnold M Kinkead
Primary Examiner
Art Unit 2817

Arnold Kinkead
July 28, 2004